

FIG. 1A

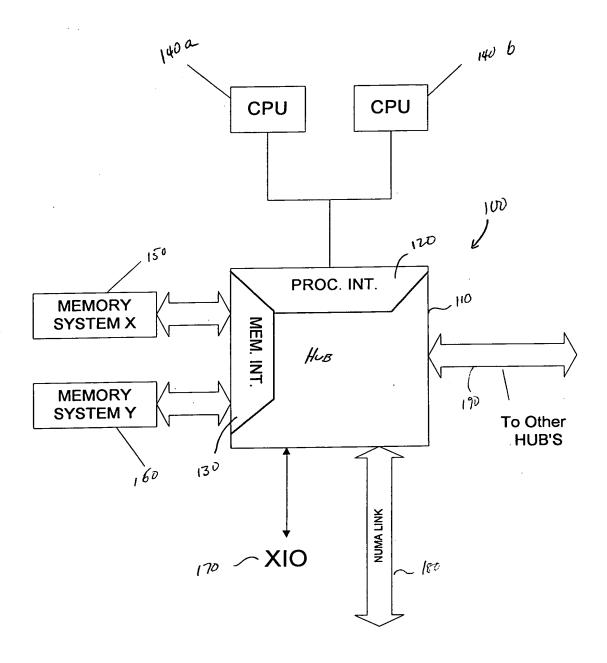


FIG. 1B

QUEUE CIRCUIT AND METHOD FOR MEMORY ARBITRATION EMPLOYING SAME Inventors: Will C. Huffman Page 2 of 8 Express Mail No. EL759108956US 062986.0205

BANK 4 48-64 GB

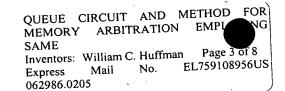
BANK 3 32-48 GB

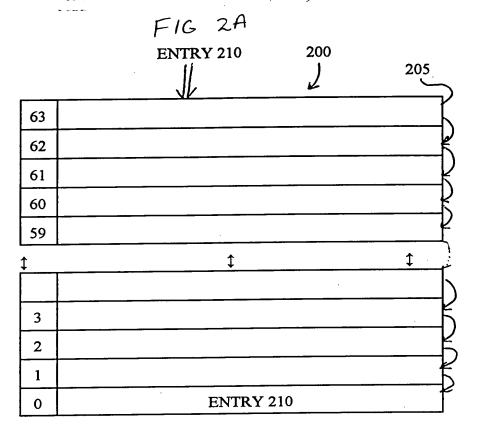
BANK 2 16-32 GB

BANK 1 0-16 GB

36 BIT MEMORY ADDRESS

BITS 35:34 - BANK SELECT BITS 33:0 - ADDRESS WITHIN BANK





63		· · · · · · · · · · · · · · · · · · ·	
62	ENTRY 290	·	_
61	ENTRY 280		- A TIND
60	ENTRY 270→IDLE		> SERVICED
59	ENTRY 260		
‡	‡	1	_
4	ENTRY 250		
3	ENTRY 240		
2	ENTRY 230		
1	ENTRY 220		
	ENTRY 210		

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Fig 2C

63	
62	•
61	ENTRY 290
60	ENTRY 280
59	ENTRY 260
‡	‡
4	ENTRY 250
3	ENTRY 240
2	ENTRY 230
1	ENTRY 220
0	ENTRY 210

				1		ENTRY	220	Ц
				0		ENTRY	210	
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£				_	11.	·		
Hand Hand			F	16	4			
STAT	`C	R/W	CHAIN	OK	BANK FREE	OP READY	TRANSACTION	
	<u> </u>	7	((_
· (, n	450	440)	430	420	410	
4	w	- (-						

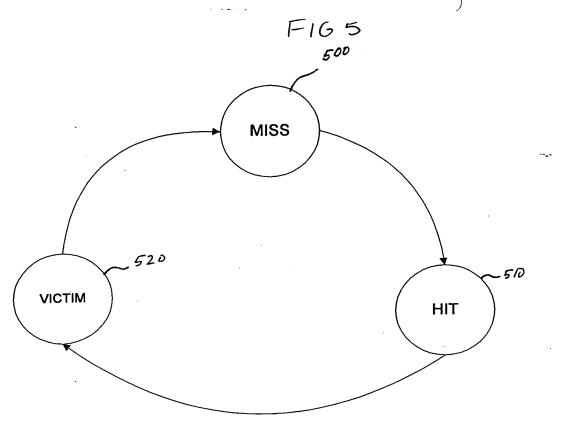
NY02:272997.1



QUEUE CIRCUIT AND METHOD MEMORY ARBITRATION EMPLO SAME

Inventors: William C. Huffman Page 5 of 8
Express Mail No. EL759108956US

062986.0205



QUEUE CIRCUIT AND METHOD FOR MEMORY ARBITRATION EMPLOYING SAME of 8 Pa Inventors: William C. Huffman No. EL759108956US

Mail Express

062986.0205

660 640 650 600 DRAM Direction Arbitration Policy Table 610 Arbitrate Direction **Follows Follows** Urgent For Threshold Write Read Write Write Read Read X X X 0 0 Write X X X x 1 0 Х Read x 0 1 0 1 Write 0 X 0 X 0 1 Read 0 0 X ō X 1 1 Write 0 1 0 0 1 1 Read 1 1 0 0 1 1 Write X x 0 1 X 1 Read 0 0 1 1 x 1 Write 1 0 1 1 x 1

